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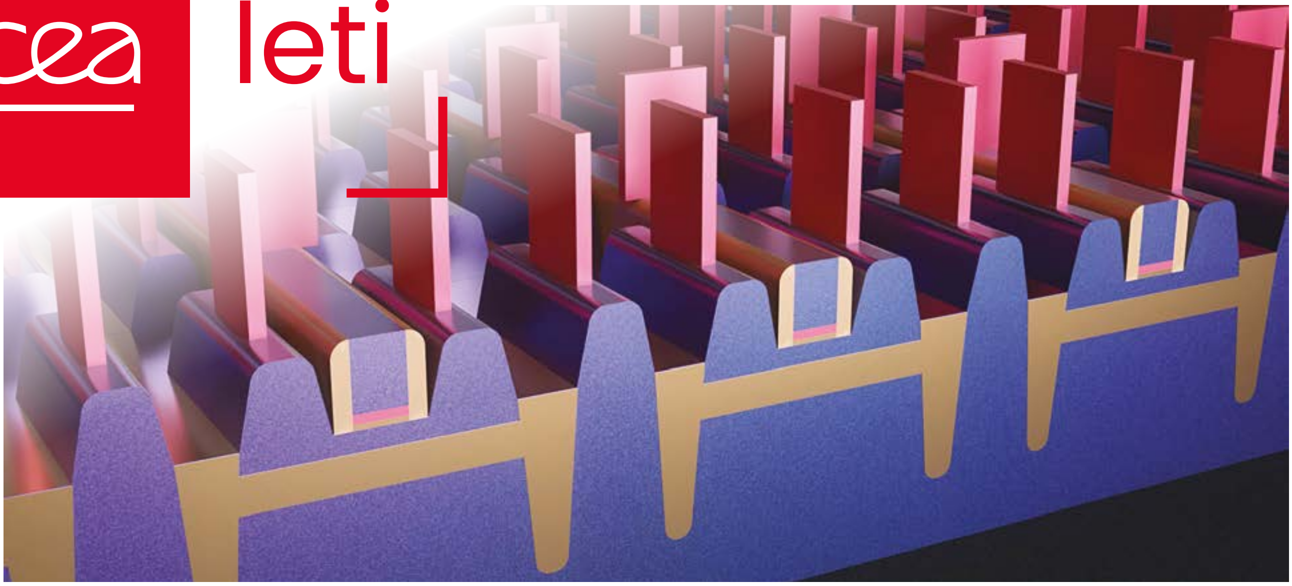


FD-SOI Next Generation 10-7 nm

An innovative generation of chips offers the best balance in Power, Performance, Area and Cost (PPAC) for highly energy efficient applications

What is it?

Already used in mobile electronics, the automotive industry and the Internet of Things, 28-18 nm FD-SOI transistors are currently produced in volume by foundries such as STMicroelectronics, GlobalFoundries and Samsung. The switch to the 10 nm node will enable very significant gains in terms of:

- Transistors density
- High-performance/low-power trade-off: circuit performance and power consumption will be modulated by back-biasing according to application needs
- Radiation resistance
- Reduced current leakage
- Manufacturing costs

Applications

FD-SOI technology can be found in the world's three major markets:

- **Communication**: 5G and sub-6 GHz smartphones, network infrastructures, components for cybersecurity
- **Automotive industry**: radar and lidar, microcontrollers
- **Smart Devices**: Internet of Things, watches and ultra-low-power connected devices, components for embedded artificial intelligence

And also in components for the space industry.

This construction project benefits from a government grant managed by the Agence Nationale de la Recherche (French National Research Agency) as part of the France 2030 under the reference "ANR-22-NEXG-0001".

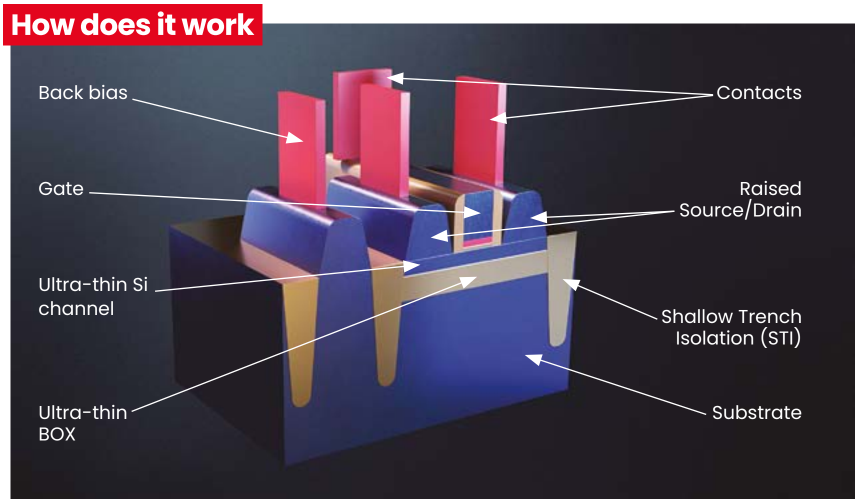
What's new?

The development of 10nm FD-SOI involves major advances in terms of substrates, the application of mechanical constraints on materials and devices, miniaturization, innovative lithography and etching processes, polarization flexibility on the back of components (back-biasing), etc.

Improving the performance/consumption trade-off is of particular interest to the smartphone market in order to improve autonomy and/or enhance functionality.

For automotive applications, the integration of non-volatile phase-change memory in the microcontroller back-end will improve reliability, storage density and performance.

How does it work



What's next?

As part of the NextGen project, CEA-Leti is investing heavily in human resources, equipment and buildings to develop 10 nm FD-SOI, while anticipating the specific needs of European microelectronics players.

The institution has already established a number of design rules. The industrial transfer of this new node will begin in 2027.

Key figures

- Metal Pitch: Minimum distance between the center of two interconnection lines is 48 nm (90 nm in FD-SOI 28 nm)
- CPP (Contacted Poly Pitch): Minimum distance between the center of two gates is 68 nm (114 nm in FD-SOI 28 nm)

Benefits as compared to FD-SOI 28 nm:

- Fourfold increase in transistor density
- At equal speeds, operating power consumption reduced by a factor of five
- At equal power, twice as fast

Key facts

- Forty years ago, the FD-SOI adventure was born at CEA-Leti laboratories in Grenoble, the heart of the French Alps.
- Over 150 patents have been filed in relation to FD-SOI.

Interested in this technology?

Contact:
Vincent Barral
vincent.barral@cea.fr
+33 632 696 330

CEA-Leti, technology research institute
17 avenue des Martyrs, 38054 Grenoble Cedex 9, France
cea-leti.com

@CEA-Leti

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