

Next generation hybrid bonding

An enabling technology for new architectures

What is it?

For more than 10 years, CEA-Leti has participated in the public-private French Nanoelec ecosystem, which represents 22 core partners. To deliver advanced packaging and die-to-wafer hybrid bonding, CEA-Leti partners with equipment manufacturers (SET, EVG, etc.) and adapts specific die-to-wafer processes from pick and place technology to self-assembly for improved throughput and alignment accuracy.

Tech highlights:

- Mastery of surface cleanliness and control of nanotopography
- Die size: 1 × 1 mm² to 10 × 10 mm²
- Inter-die spacing: down to 40 µm inter-die spacing
- Interconnection pitches: from 10 μm to less than 5 μm
- · Electrical yield: more than 90% electrical yield

Applications

- Chiplet integration for HPC (high performance computing), edge IA or optical computing
- Future memory
- · Photonic devices
- Imagers
- Lighting
- Displays
- · Radio frequency

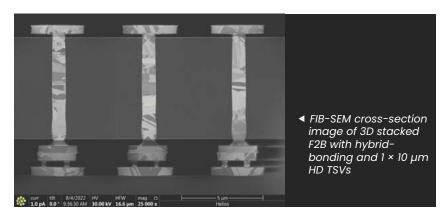
Work performed in the frame of the IRT Nanoelec consortium.

What's new?

CEA-Leti offers 3D integration with improved functions and performance thanks to several technical advances:

- Various circuits (top-die & bottom-die) can now be hybrid bonded to improve interconnection and reduce pitches
- Top-die circuits can be joined to a substrate using TSVs to connect signals and the power supply
- Heterogeneous bonding techniques enable the combination of various new substrates

CEA-Leti is also working on new integration technologies such as self-assembly. This advance enables higher alignment performance (+/-200 nm) and increased throughput (thousands dies/h).



What's next?

- Reduced pitch interconnection
- Reduced temperature
- Multi-stack die-to-wafer processes
- Industrial transfer

How do we work together?

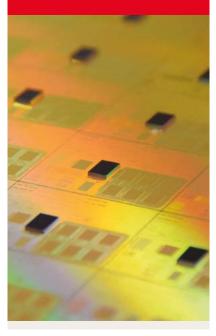
CEA-Leti's advanced platforms enable partners to:

- Develop process modules that are too disruptive for existing fabs
- Facilitate mass manufacturing for specific designs that are optimized at the research level but not yet compatible with large-scale operations
- Co-create new functions for a given application

Key facts

Technological advances supported by cutting-edge research with:

- An Outstanding Interactive Presentation Paper (ECTC 2022)
- Papers published in ECTC 2022 and ESTC 2022
- Seven papers presented to ECTC 2023
- A cover story by Chip Scale Review (Oct. 2022)



Interested in this technology?

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